

**GOVT. ENGINEERING COLLEGE AJMER**  
**Department of Electronics & Communication Engineering**

Ref. No. GECA/ECE/2018/1338

Date: 28/09/2018  
01/10/2018

**I -Mid Term Test (Main/Back\*/Old Back\*), 2018-19**

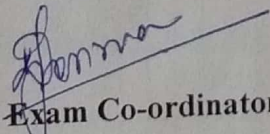
Date	<i>B. Tech III Sem.</i>	Session
03.10.2018	3EC2-01 Advanced Engineering Mathematics-I	S-I
03.10.2018	3EC4-04 Digital System Design	S-II
04.10.2018	3EC4-05 Signal & Systems	S-I
04.10.2018	3EC4-06 Network Theory	S-II
05.10.2018	3EC4-07 Electronics Devices	S-I

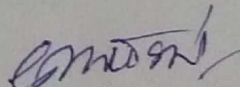
\*subjected to the completion of related formalities of exam section.

\*\*The exam of the 3EC1-02/3EC1-03 Technical Communication / Economics and Financial Accounting will be held later, which will be informed accordingly.

Sitting Plan: (S. No. 1 to 48 in NB-112, Rest all Incl. Back Students in NB-113)

Time Schedule: S-I: 10:30 - 11:30 AM      S-II: 12:30 - 1:30 PM

  
(Dept. Exam Co-ordinator)

  
(Head, ECE)

Copy to: (Information through College website/portal/mail)

- (1) Principal for kind information
- (2) Chief Coordinator (Exams.)
- (3) Concerned Department Heads
- (4) Deptt. Notice Boards,
- (5) Concerned faculty members by circulation,
- (6) Guard File

**GOVT. ENGINEERING COLLEGE AJMER**  
**Department of Electronics & Communication Engineering**

Ref. No. **II-Mid Term Test (Main/Back\*/Old Back\*), 2018-19** Date: **28/09/2018**  
*GECA/ECE/2018/1337* *01/10/2018*

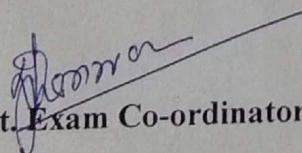
Date	<i>B. Tech V Sem.</i>	Session
06.10.2018	5EC1 SIGNALS AND SYSTEMS	S-I
06.10.2018	5EC2 LINEAR INTEGRATED CIRCUITS	S-III
08.10.2018	5EC3 TELECOMMUNICATION ENGG.	S-I
08.10.2018	5EC4 ANALOG COMMUNICATION	S-III
09.10.2018	5EC5 MICROWAVE ENGINEERING-I	S-I
09.10.2018	5EC6.1 BIOMEDICAL INSTRUMENTATION	S-III
	<i>B. Tech VII Sem.</i>	
06.10.2018	7EC1- ANTENNA & WAVE PROPAGATION	S-II
06.10.2018	7EC3 DIGITAL IMAGE PROCESSING	S-IV
08.10.2018	7EC4 WIRELESS COMMUNICATION	S-II
08.10.2018	7EC6 VHDL	S-IV

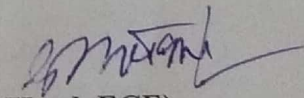
\*subjected to the completion of related formalities of exam section.

Note: II-Midterm Exam of (7EC2) Digital Signal Processing and (7EC5) VLSI Design will be held later with prior information.

Sitting Plan: (S. No. 1 to 50 in NB-112, Rest all Incl. Back Students in NB-113)

Time Schedule: S-I: 8:15 - 9:15 AM      S-II: 09:30 - 10:30 AM  
S-III: 10:45 - 11:45 AM      S-IV: 12:00 - 01:00 PM

  
(Dept. Exam Co-ordinator)

  
(Head, ECE)

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